

FIG. 1A

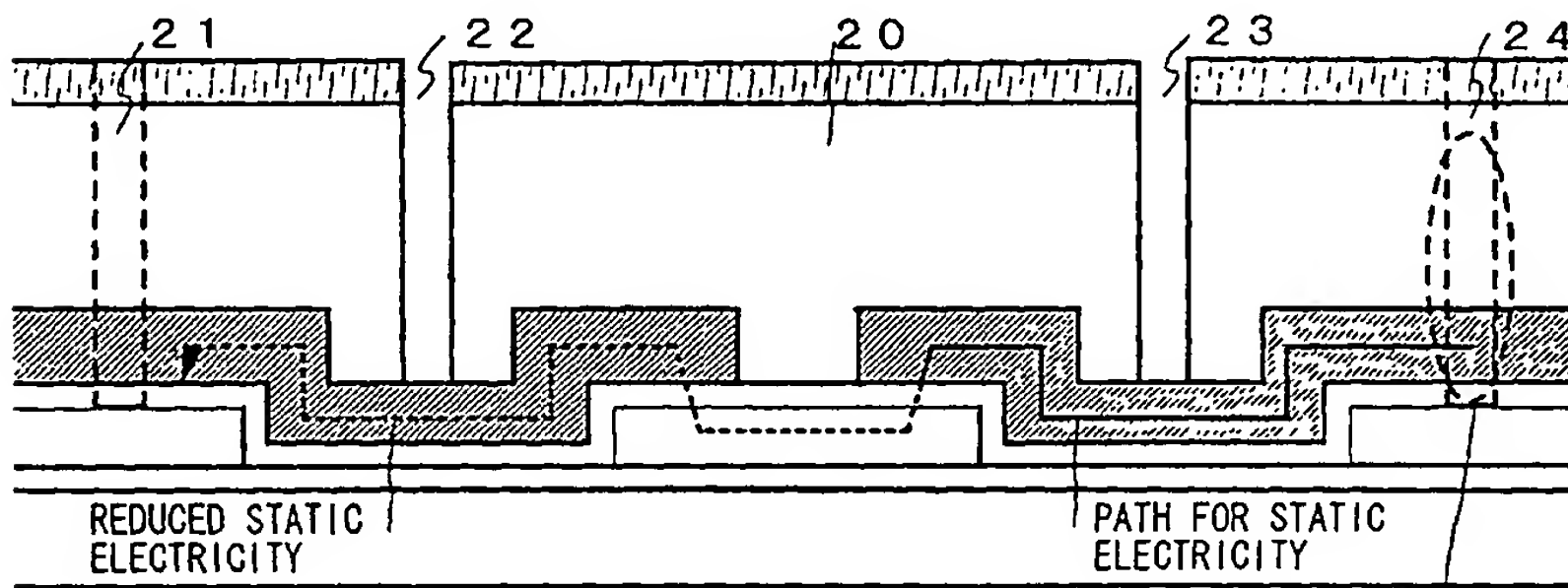


FIG. 1B

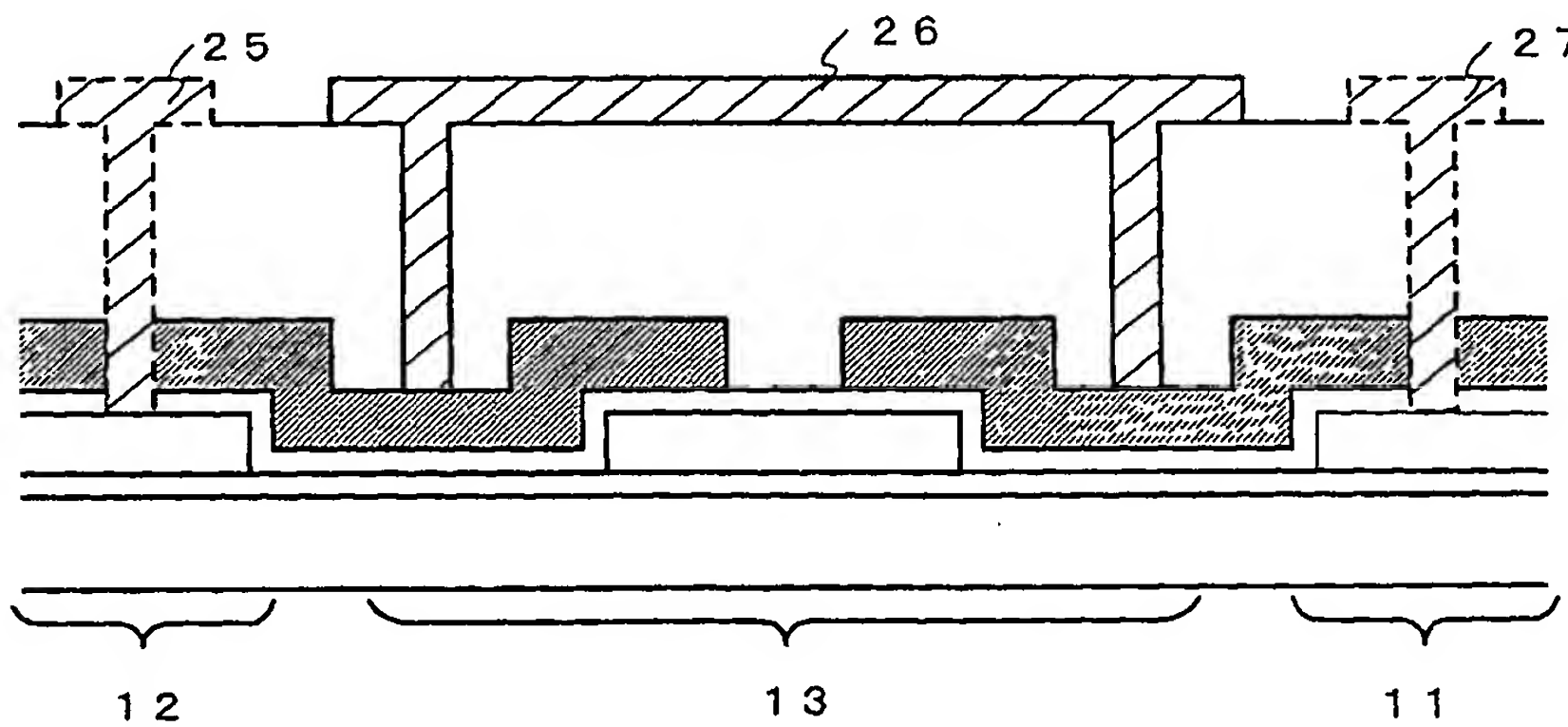


FIG. 1C

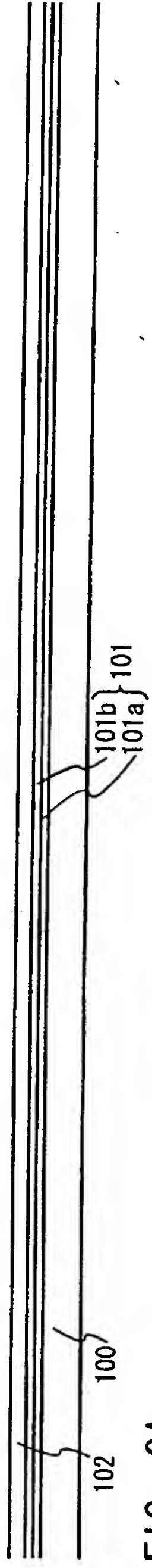


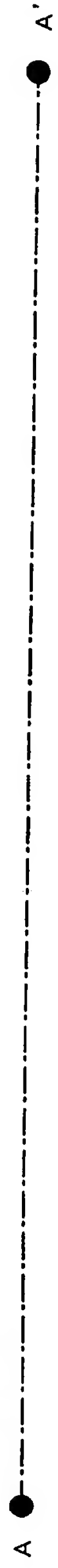
FIG. 2A



FIG. 2B



FIG. 2C



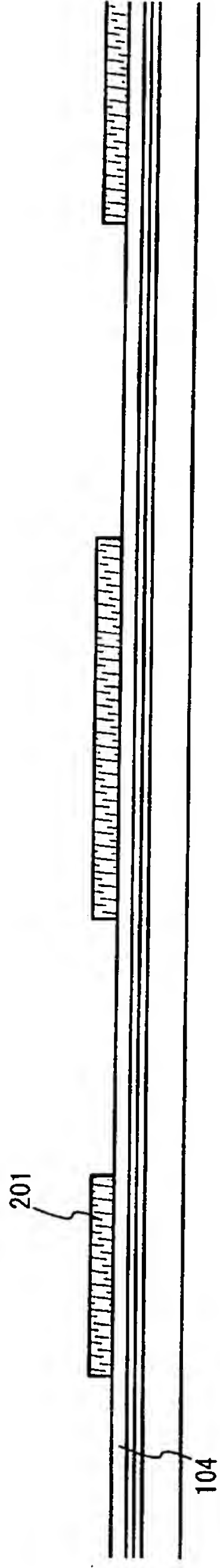


FIG. 3A

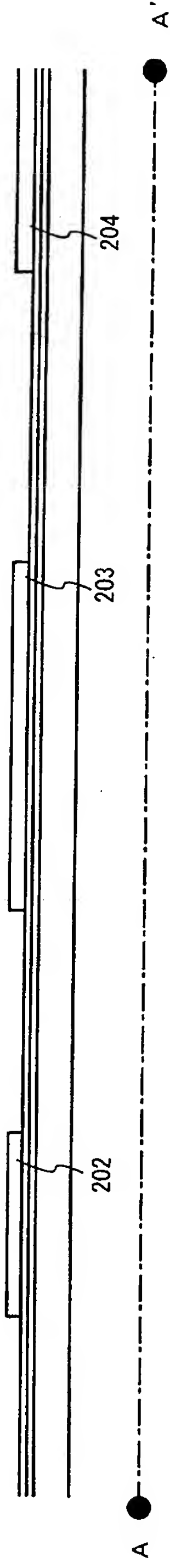


FIG. 3B

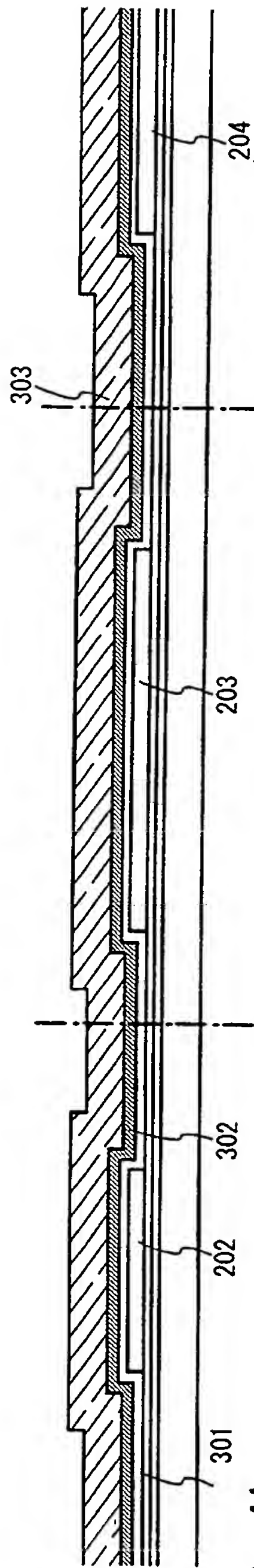


FIG. 4A

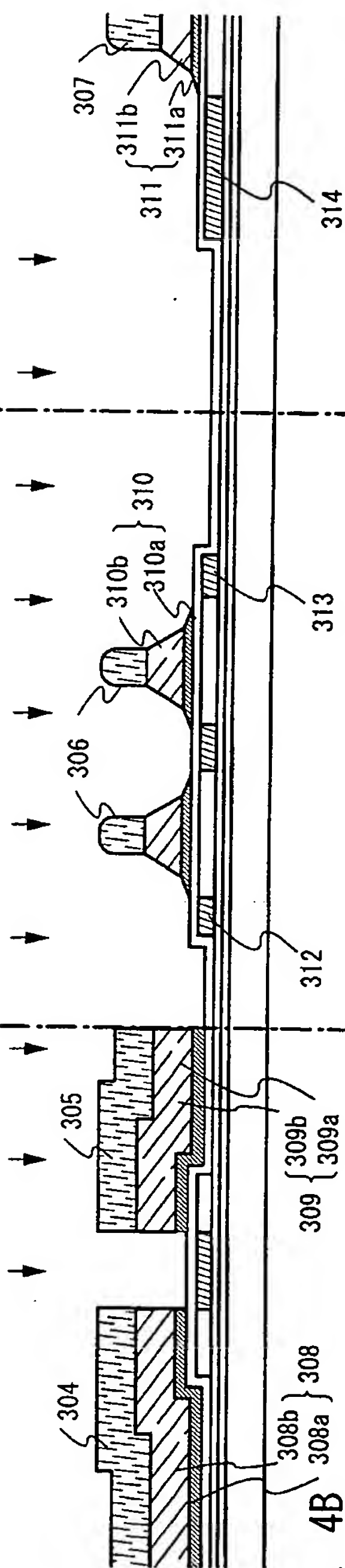


FIG. 4B

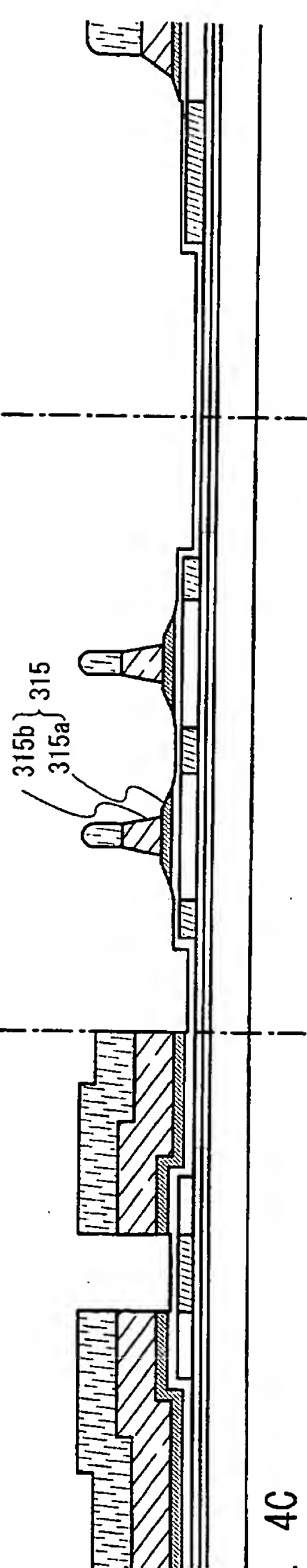
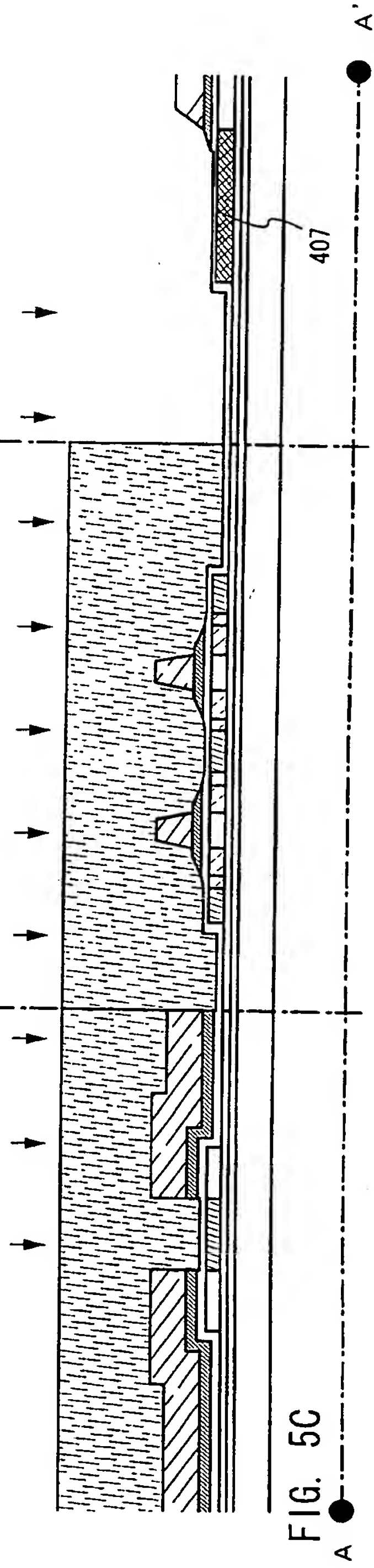
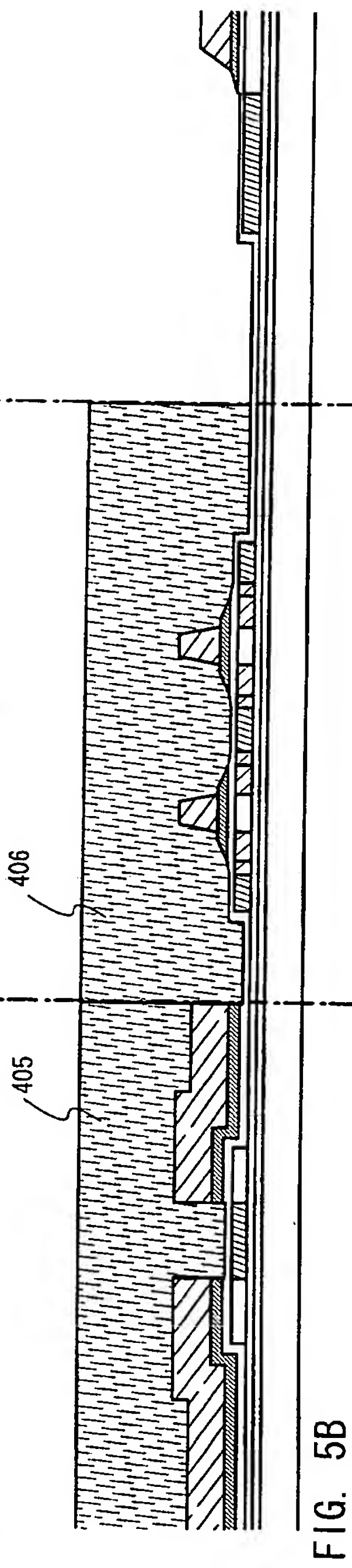
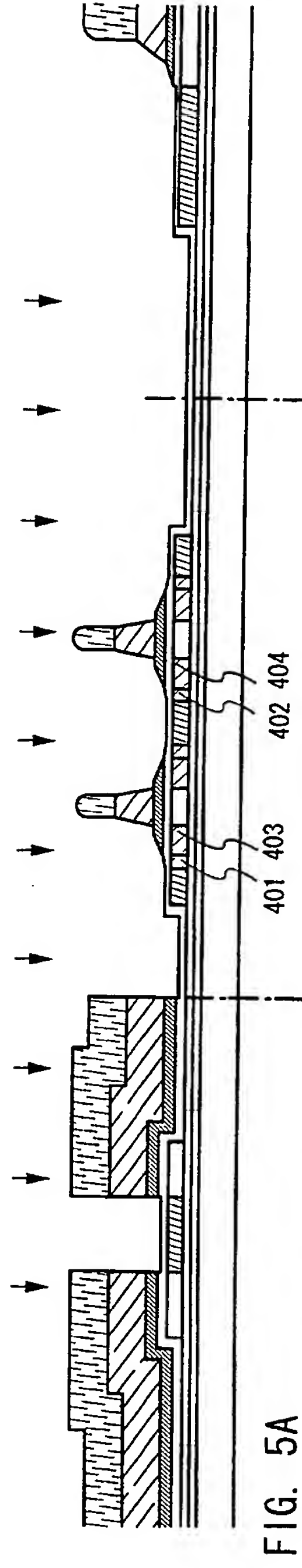


FIG. 4C

A ●-----● A'



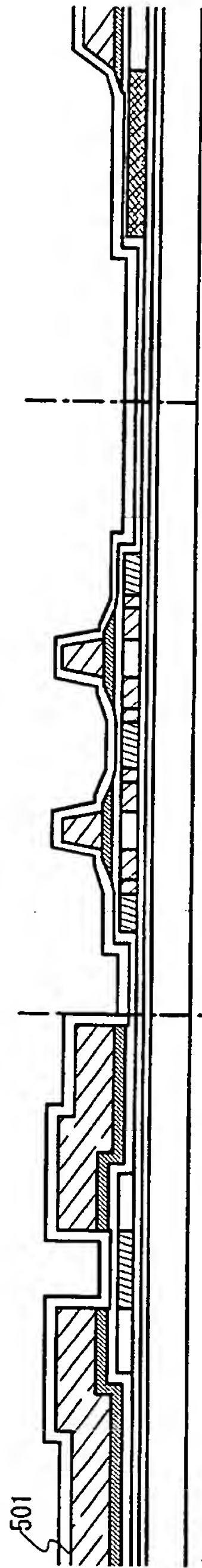


FIG. 6A

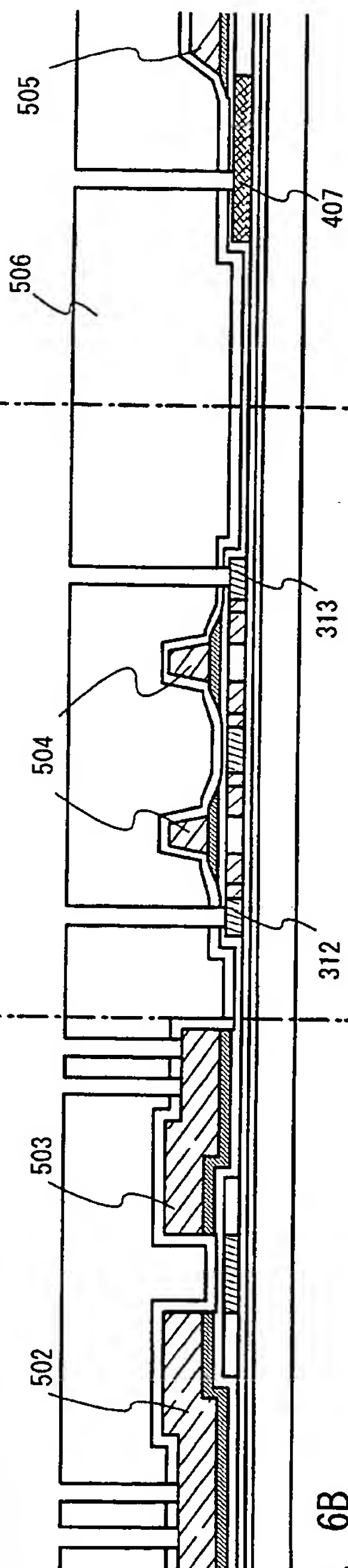


FIG. 6B

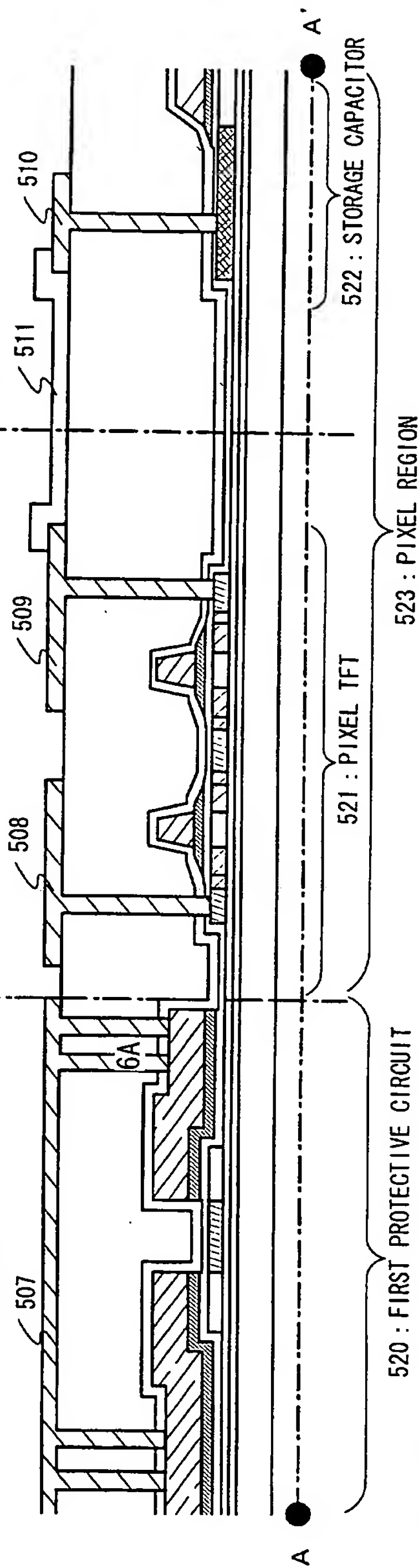


FIG. 6C

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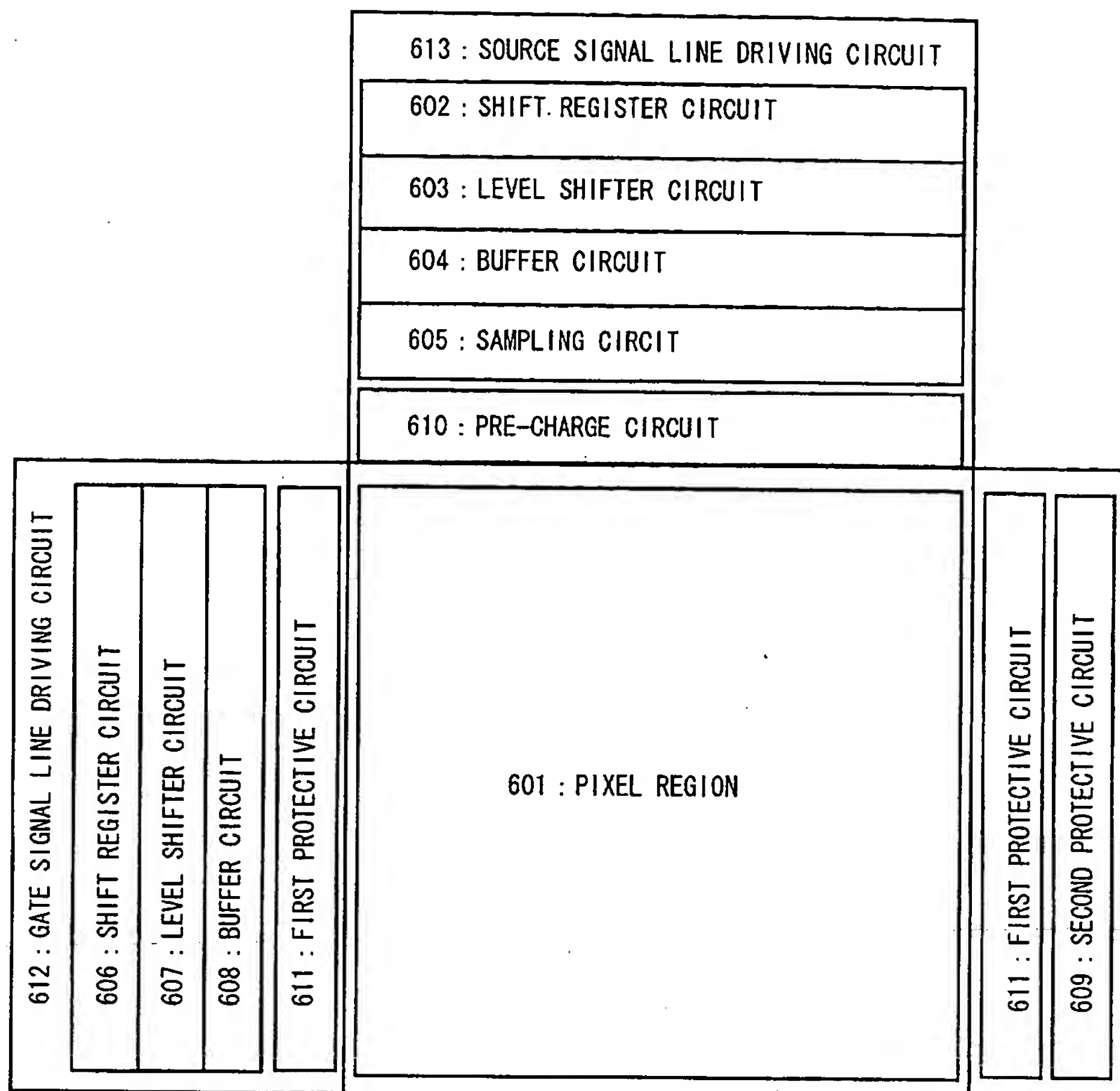


FIG. 7

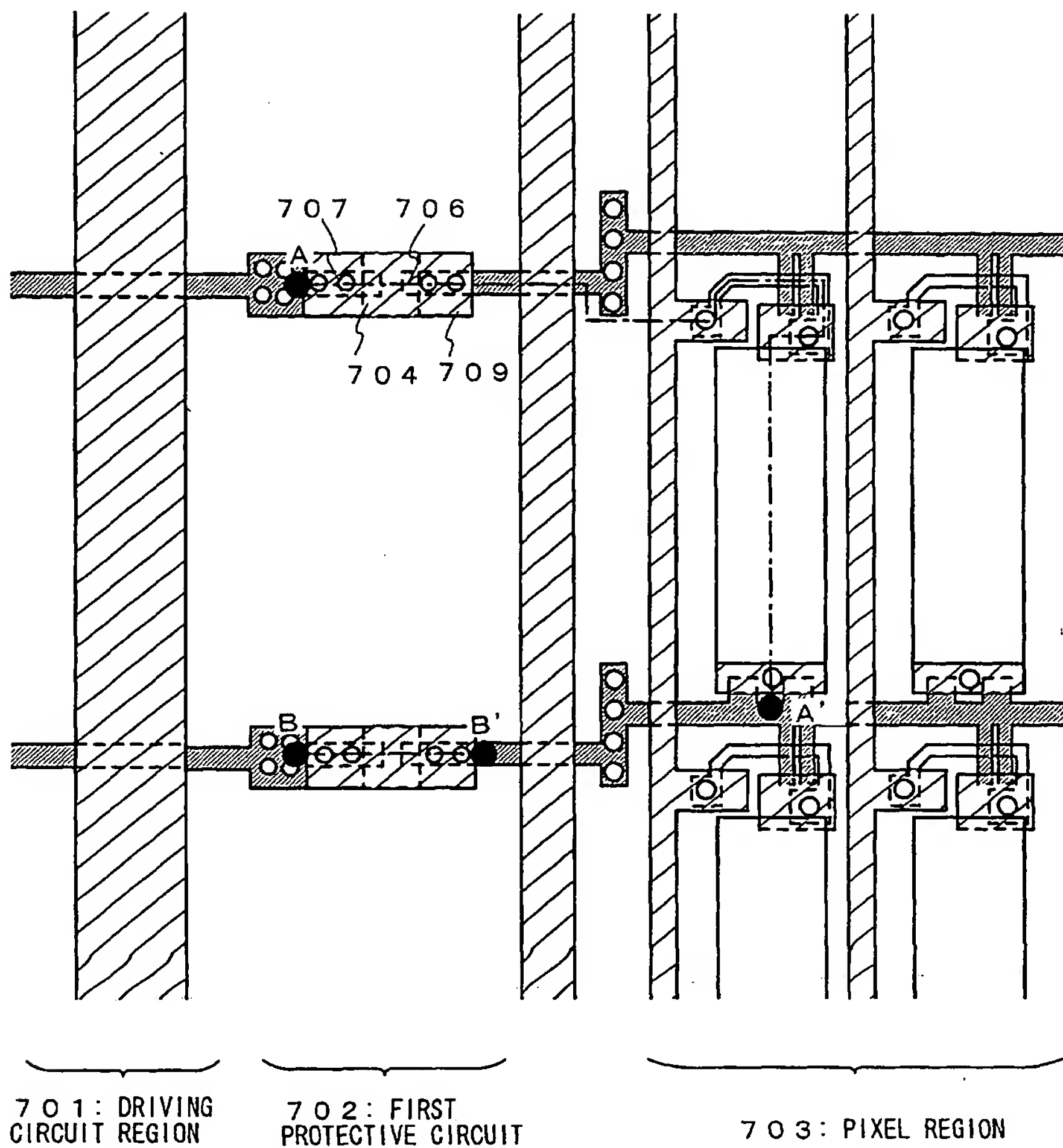


FIG. 8A

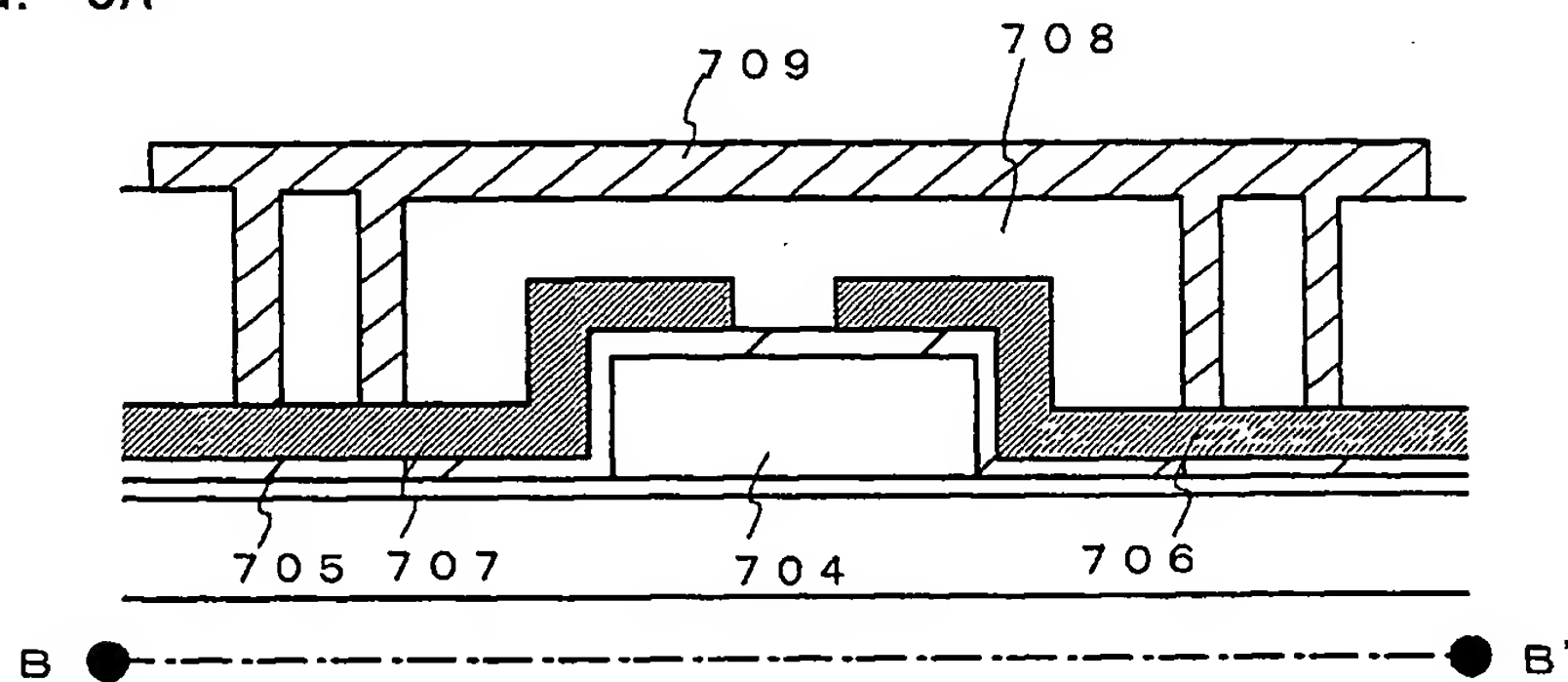


FIG. 8B



10000043-120401

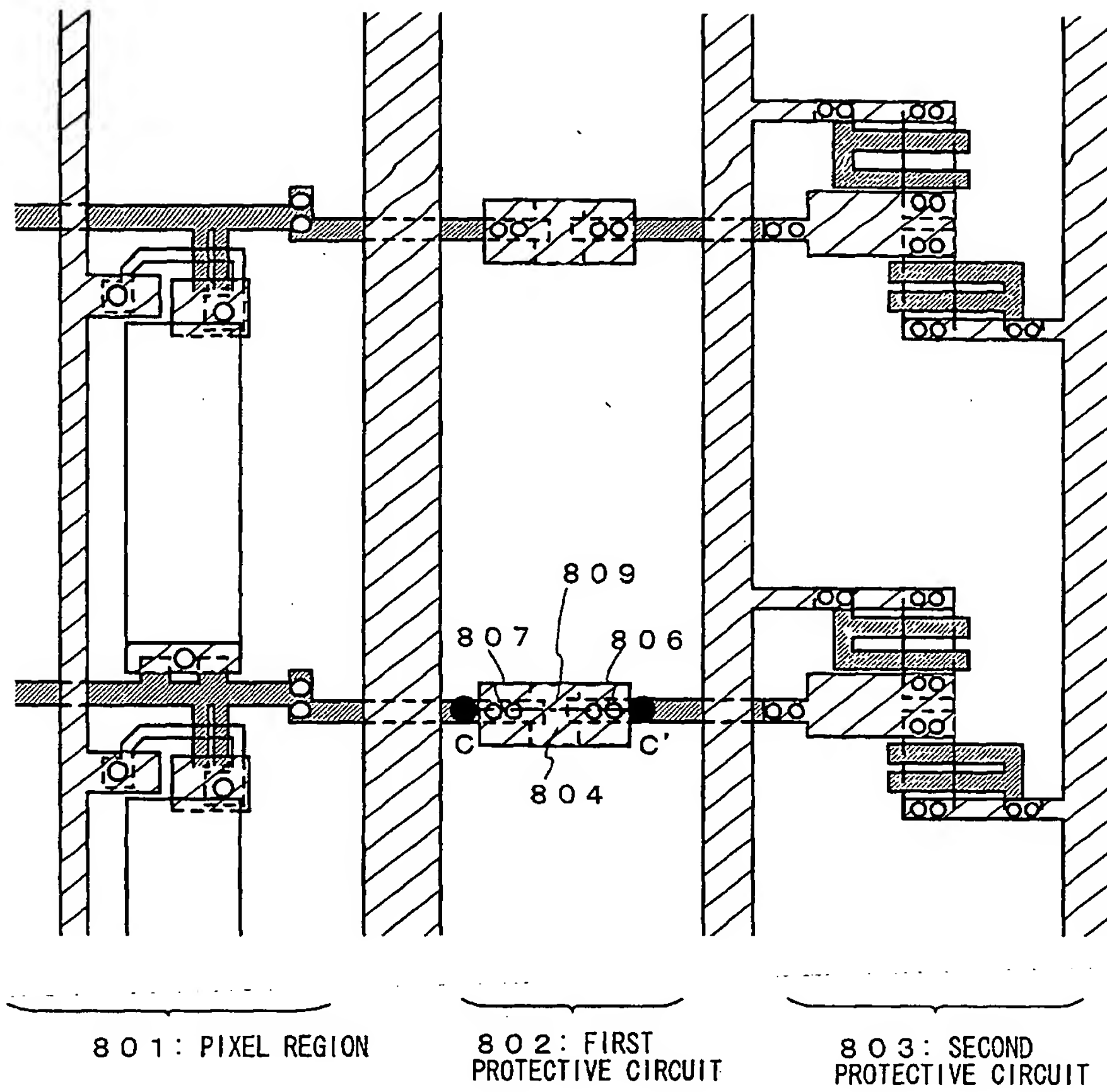
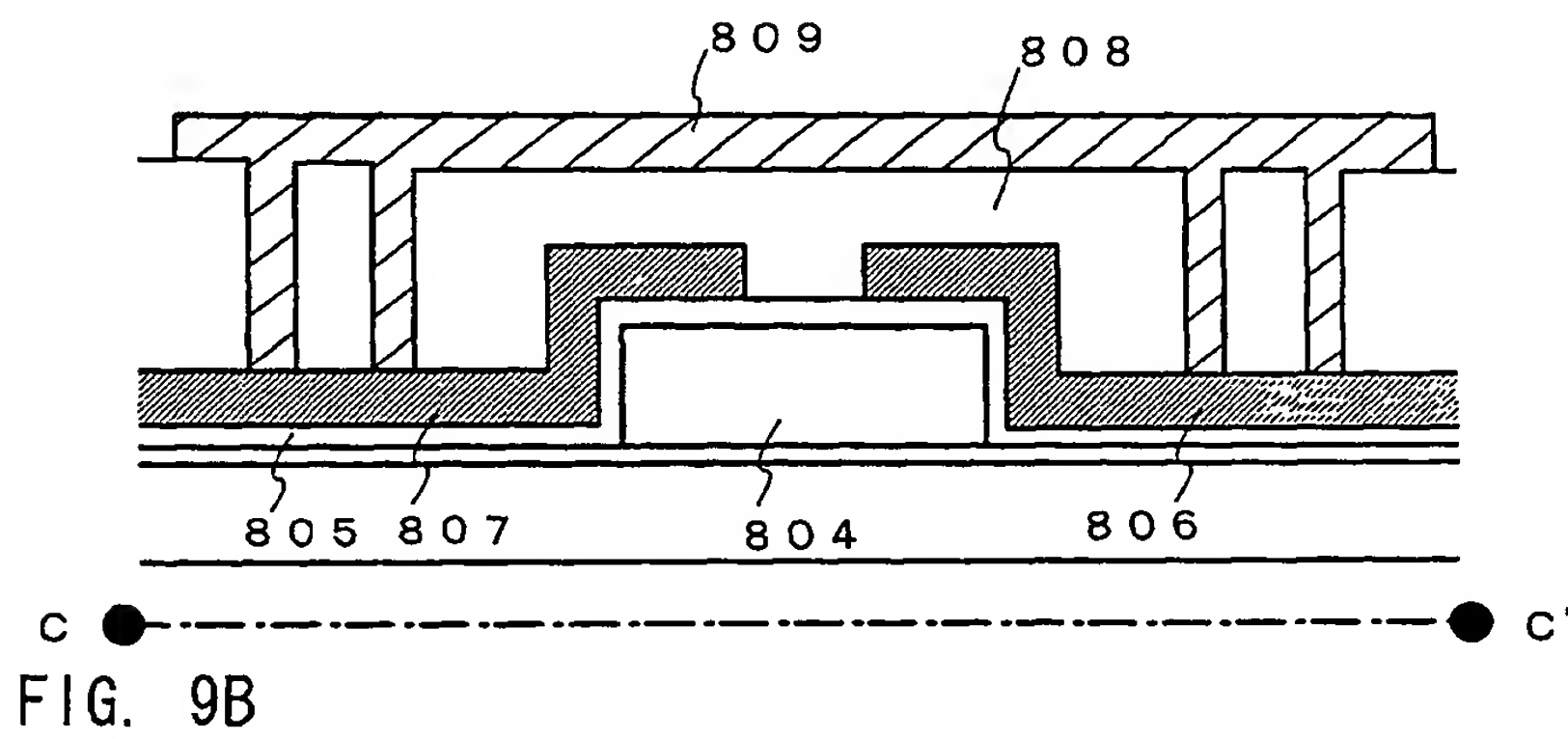


FIG. 9A



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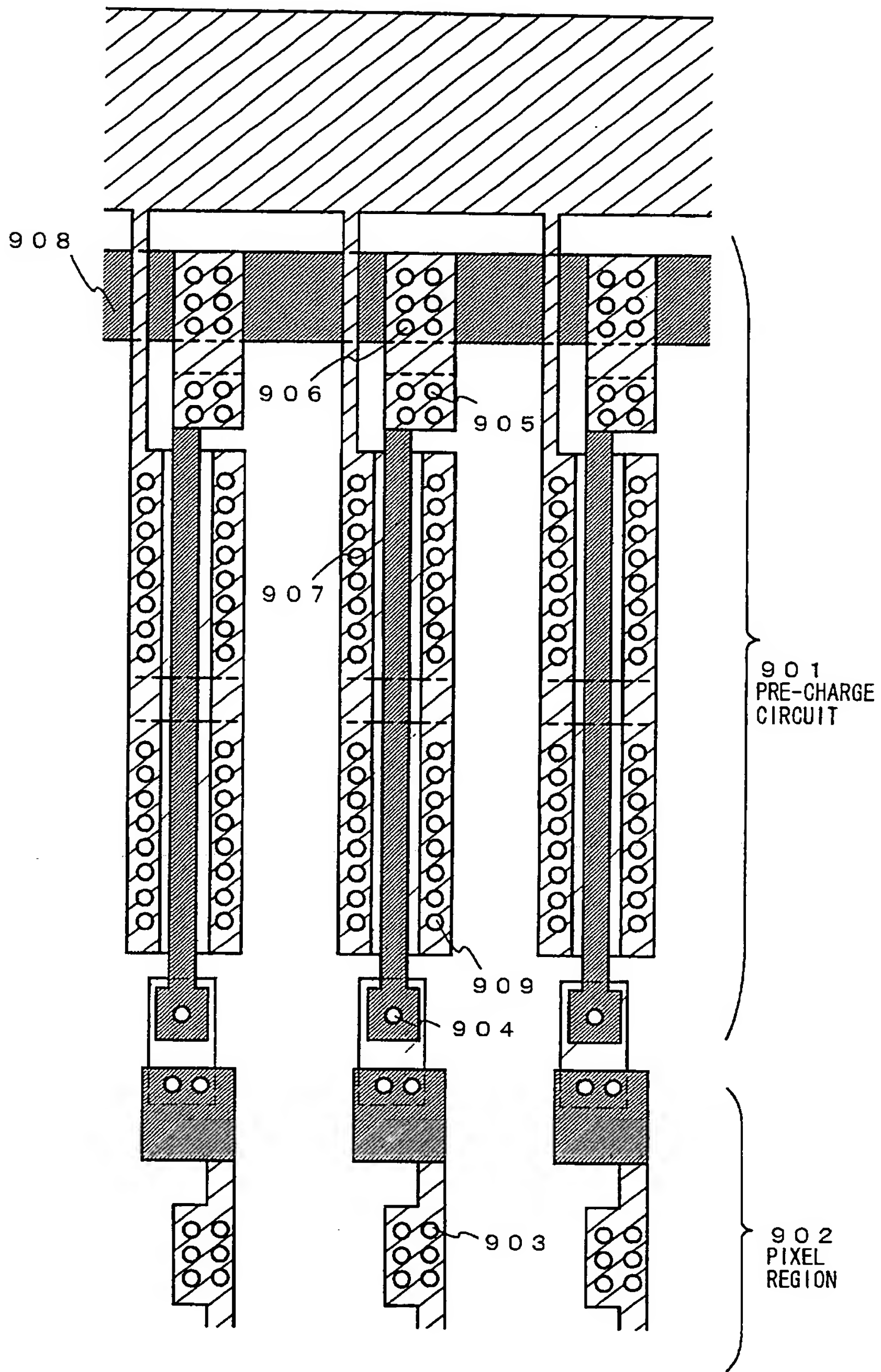


FIG. 10

FIG. 11

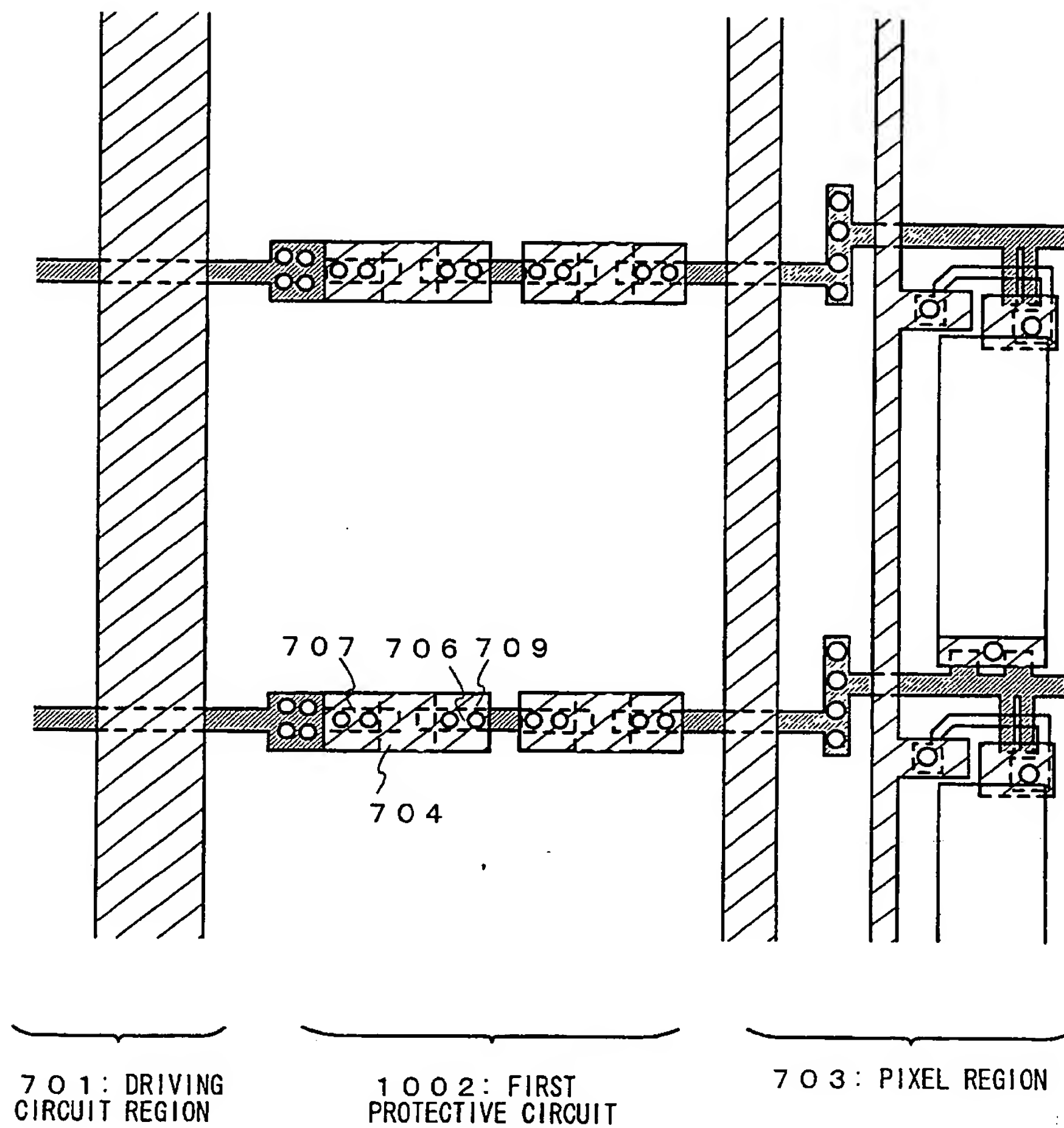


FIG. 11

FIG. 12A

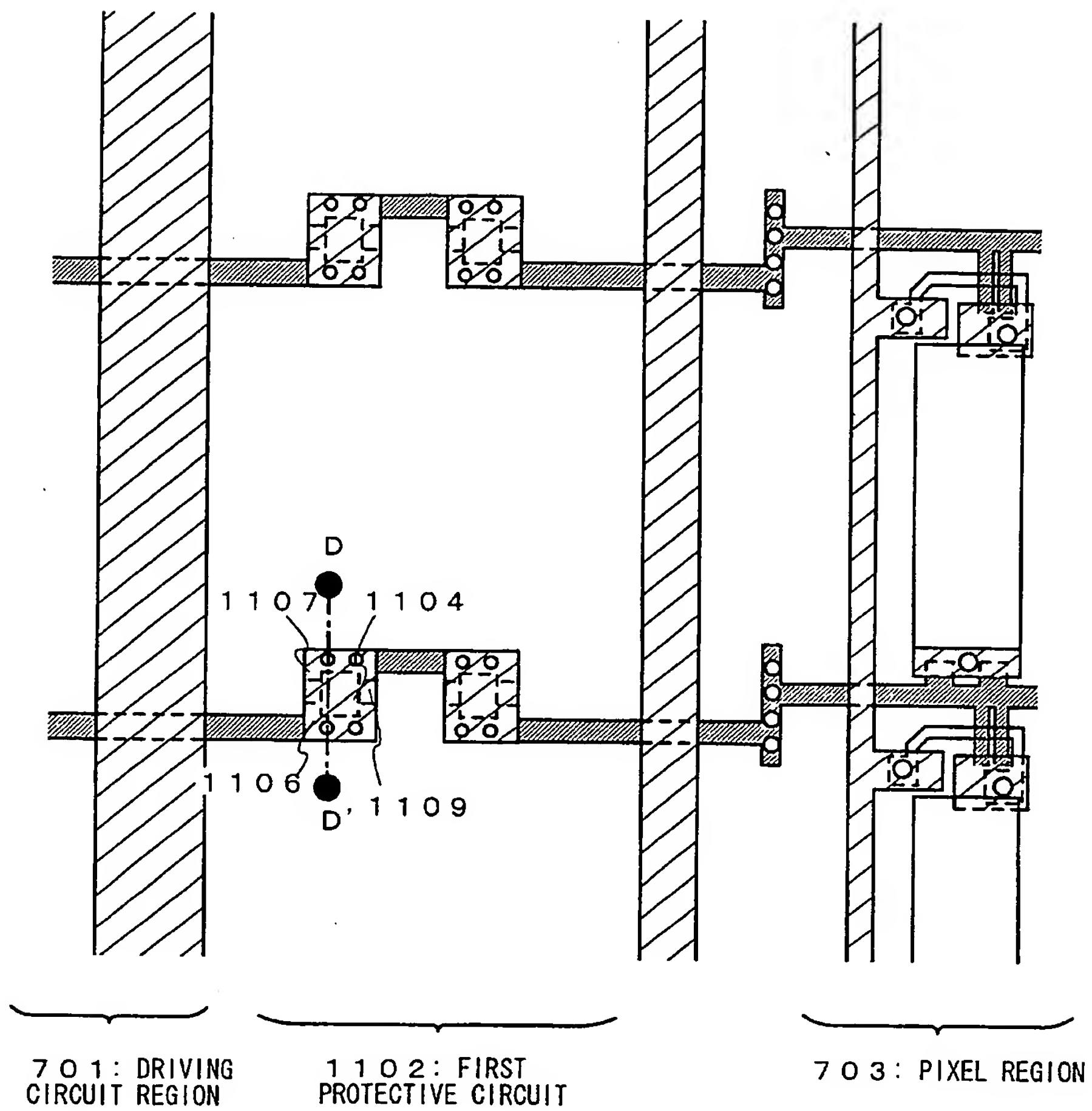


FIG. 12A

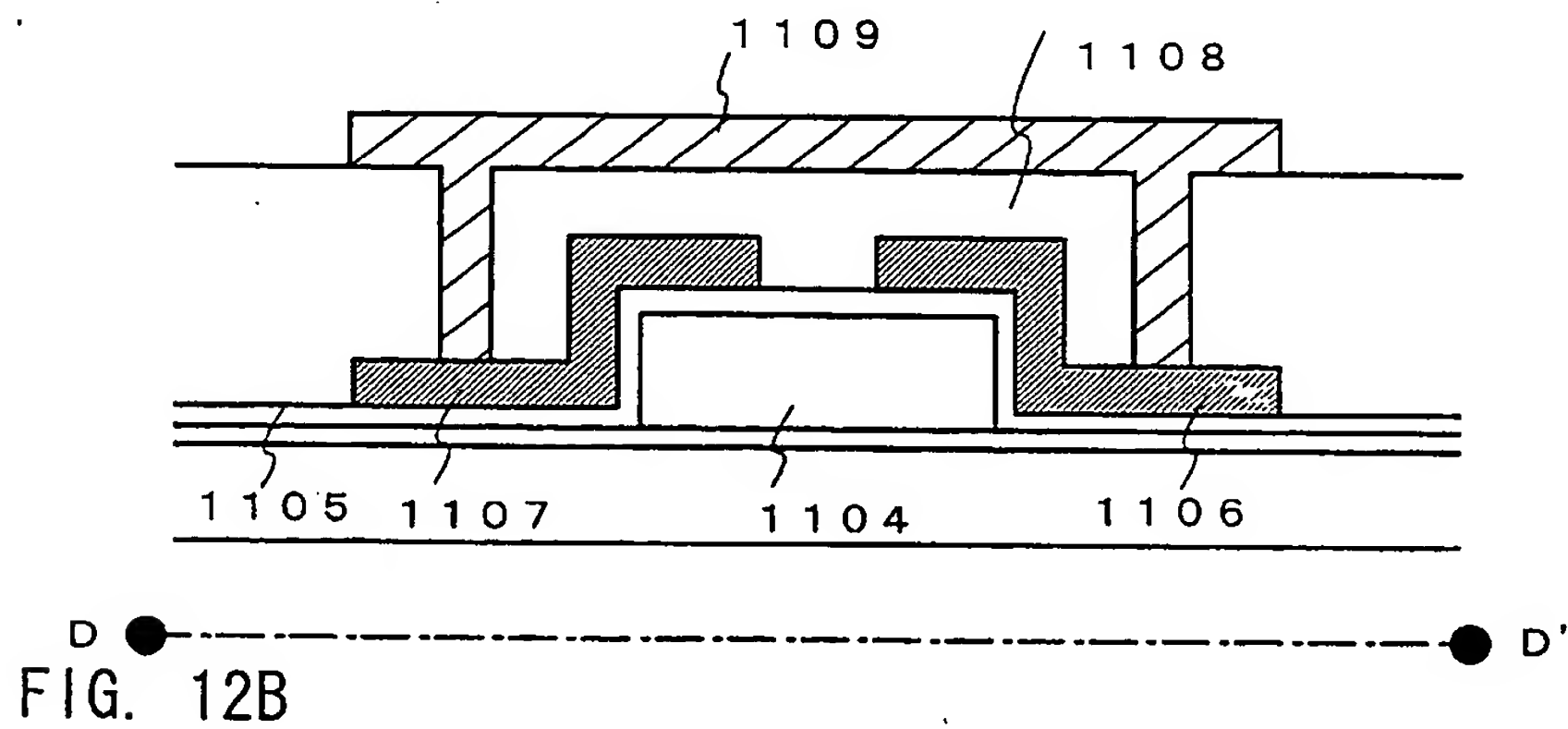


FIG. 12B

1005043-100403

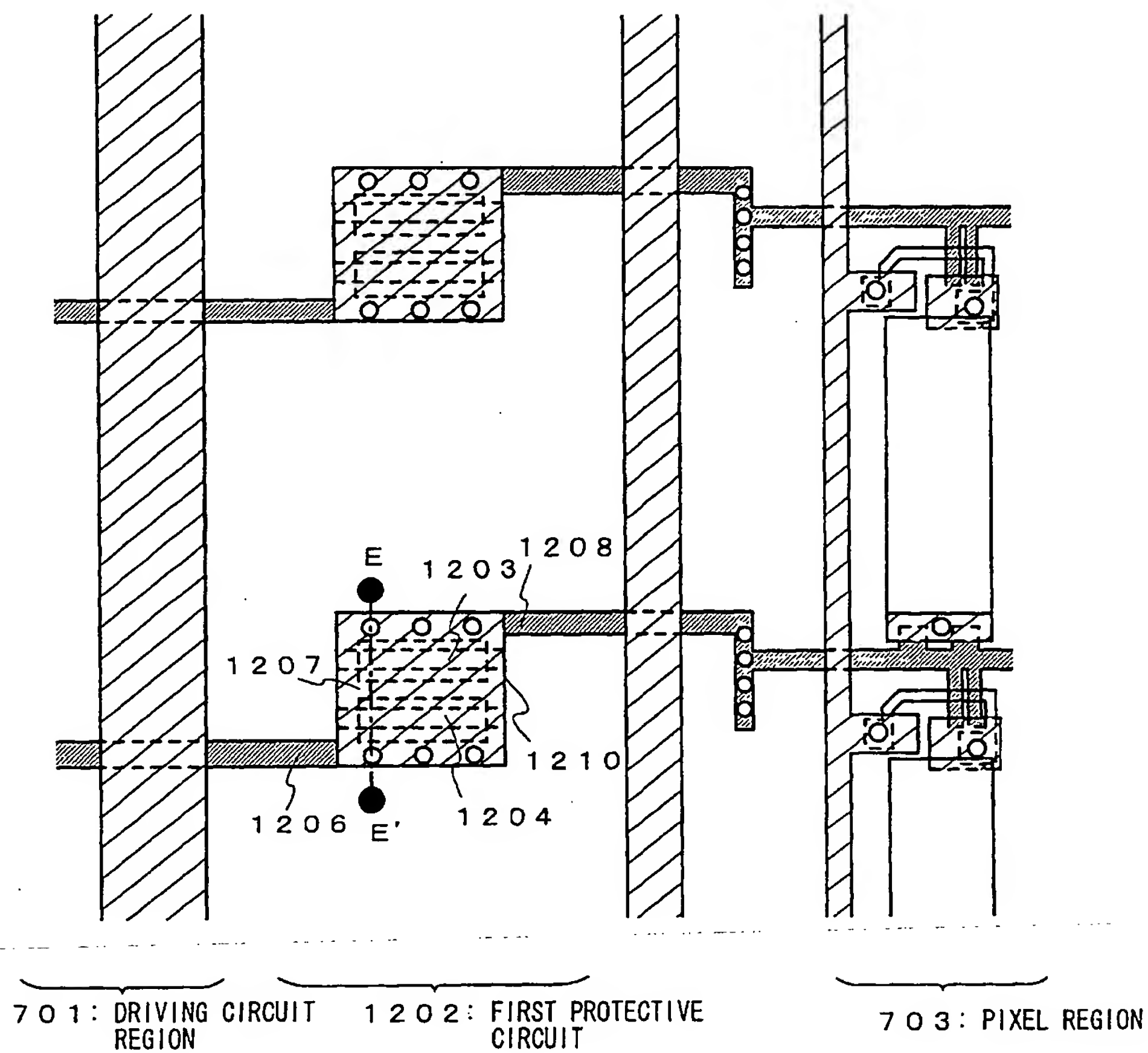


FIG. 13A

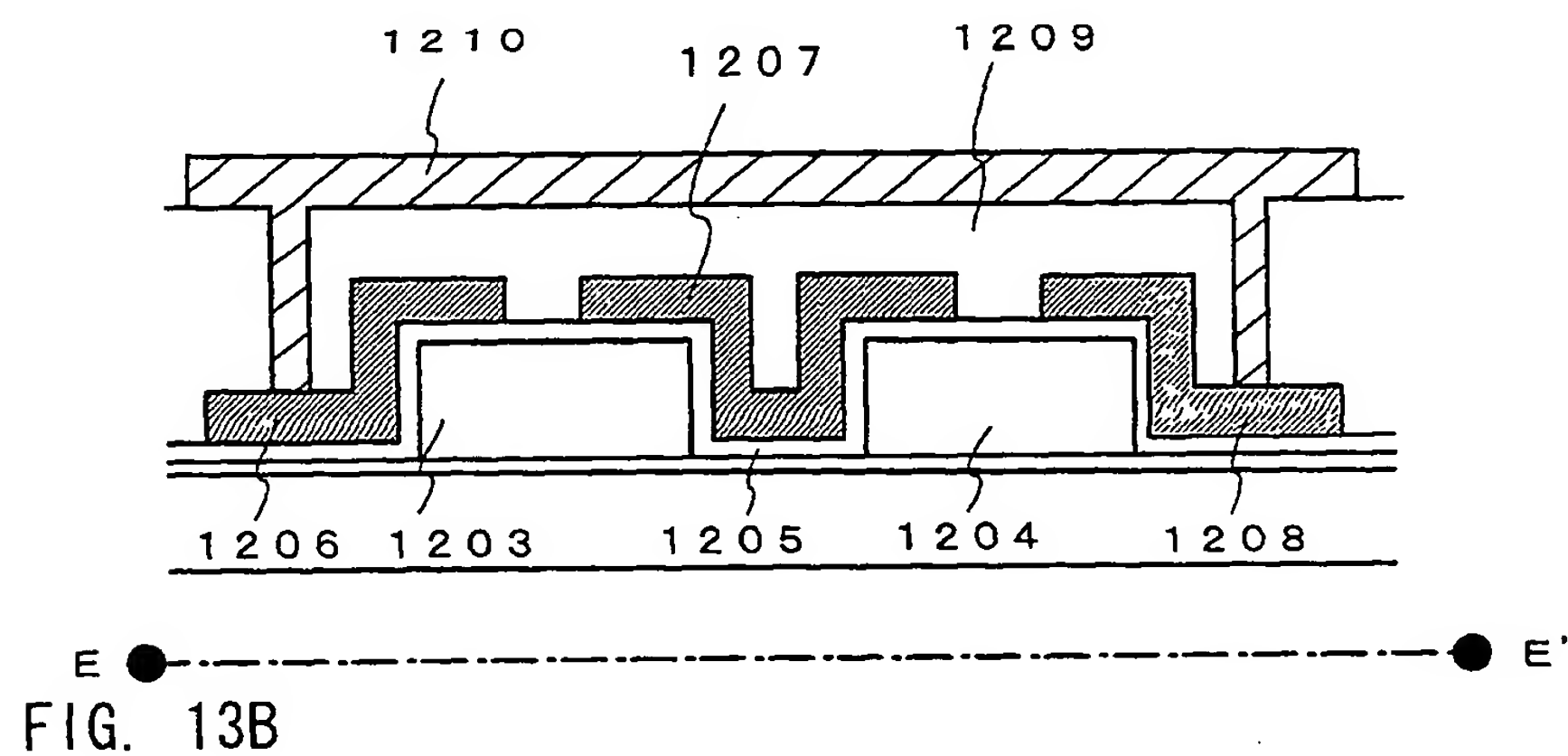


FIG. 13B

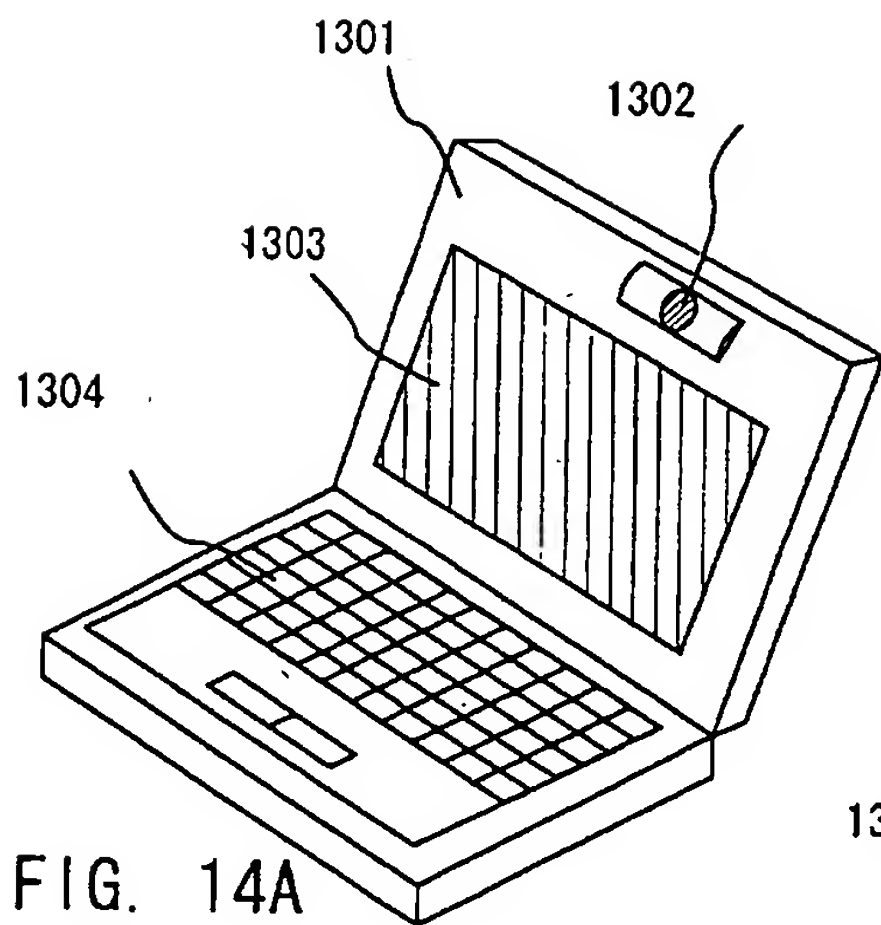


FIG. 14A

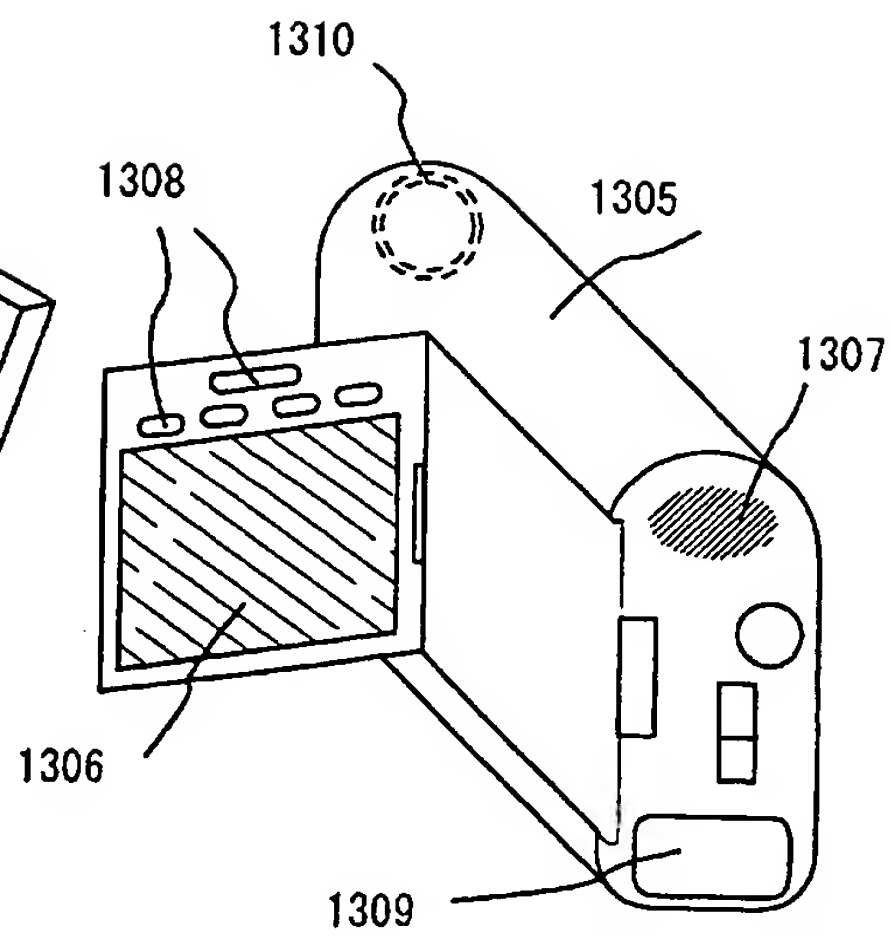


FIG. 14B

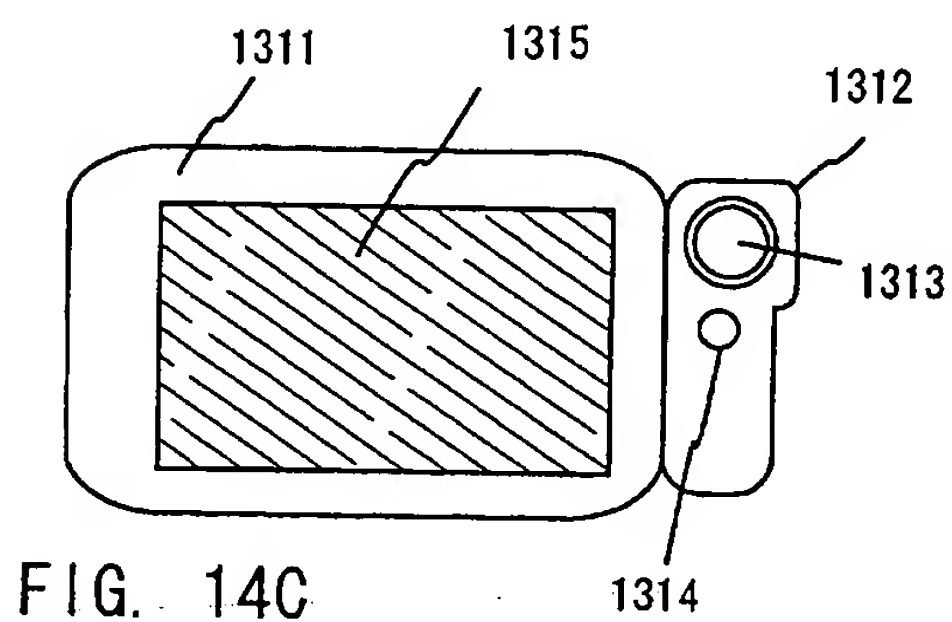


FIG. 14C

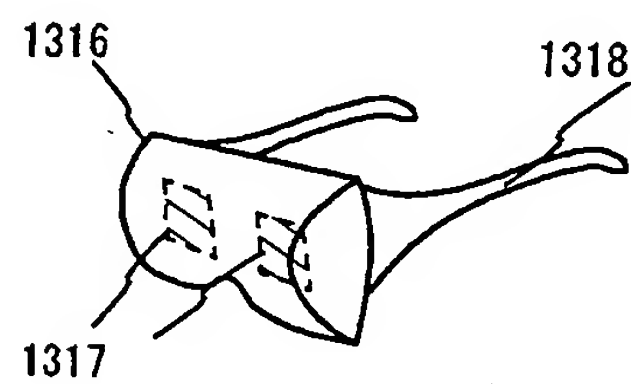


FIG. 14D

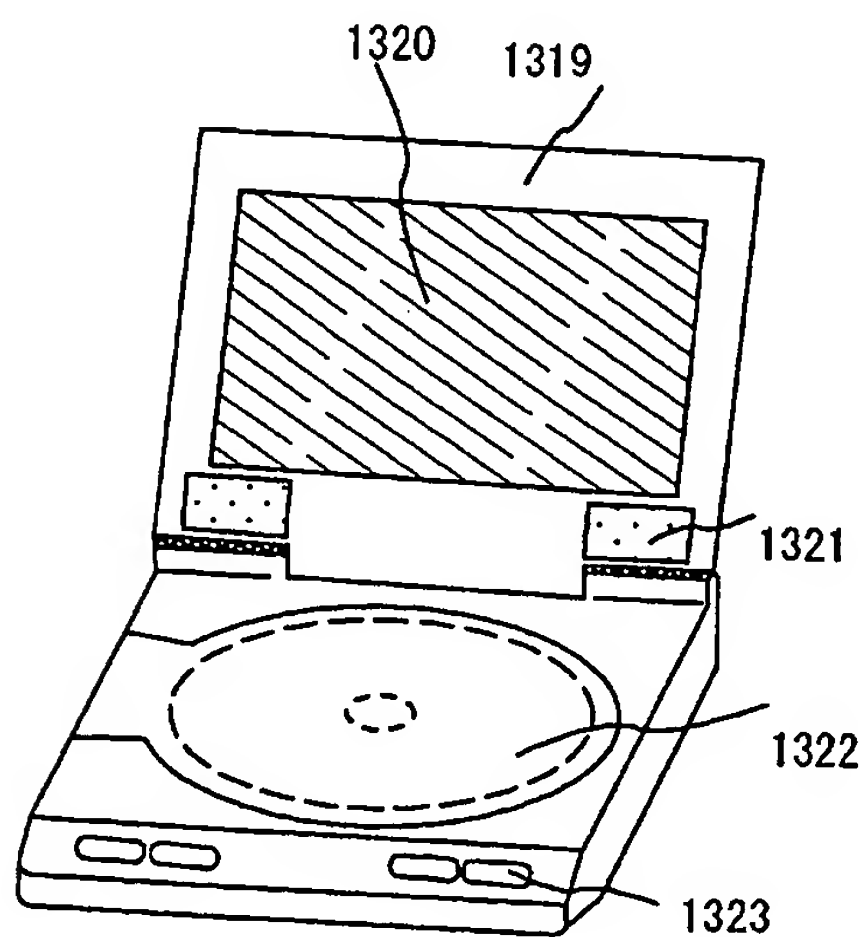


FIG. 14E

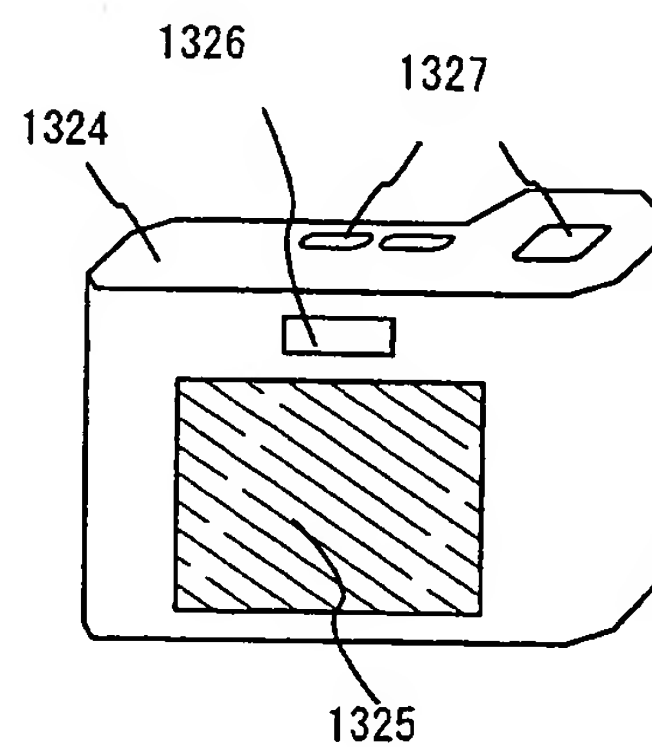


FIG. 14F

FIG. 14A

1279-th 1280-th 1281-th

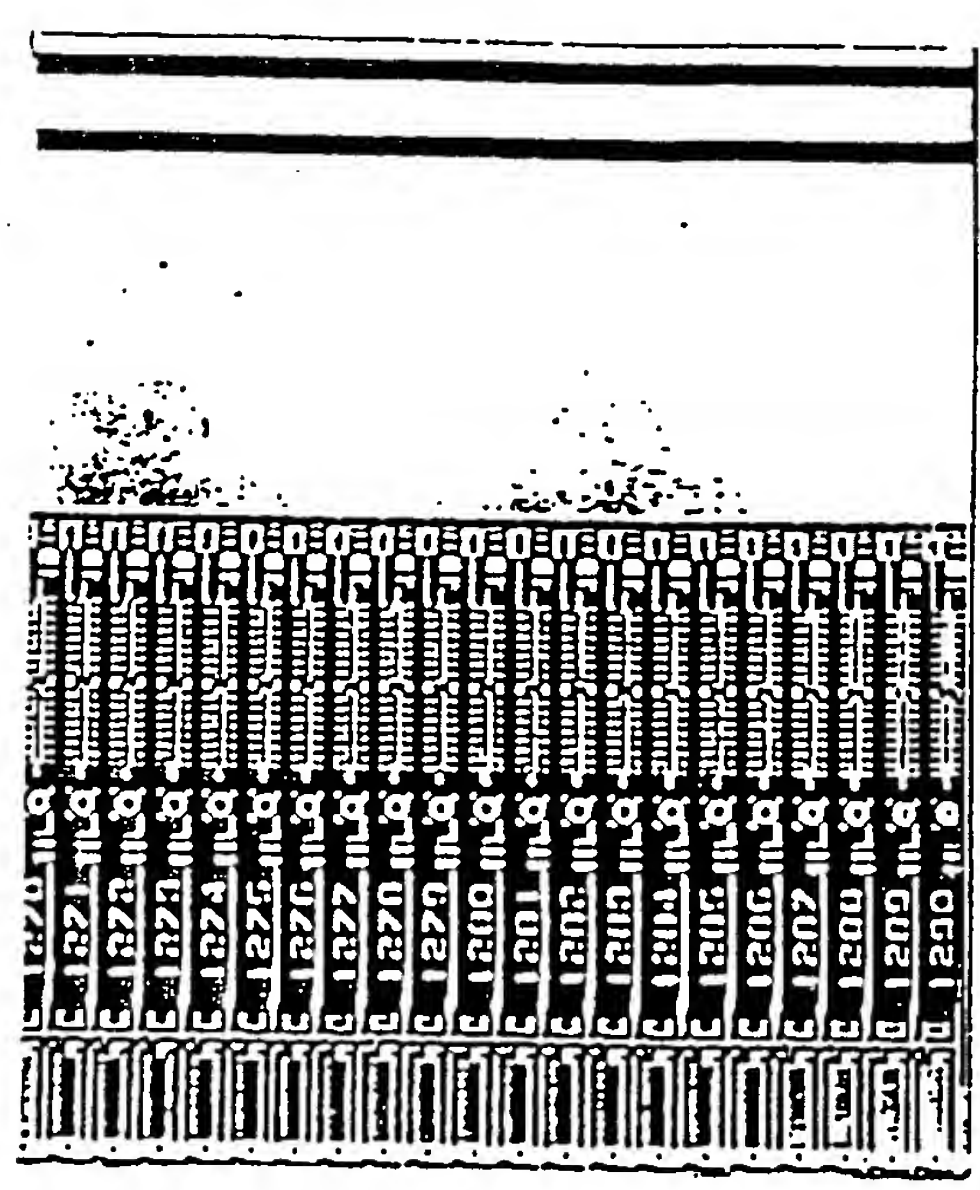


FIG. 16A

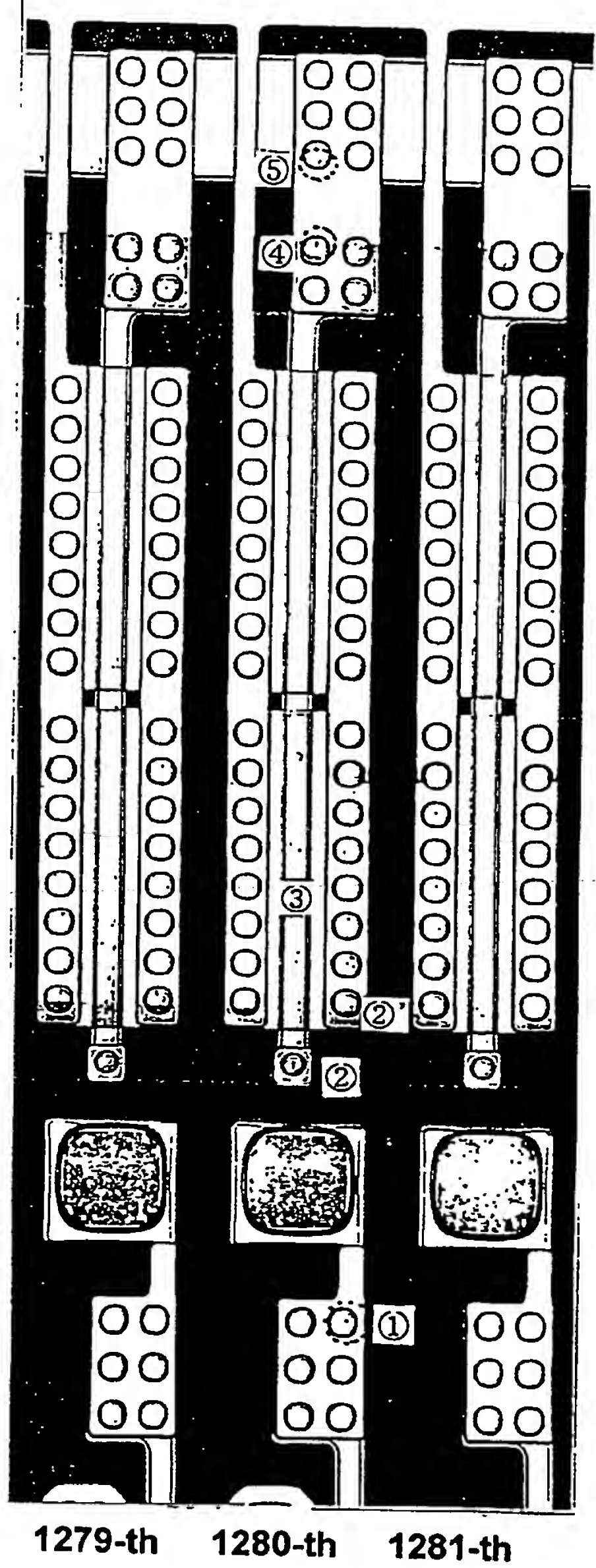


FIG. 16B

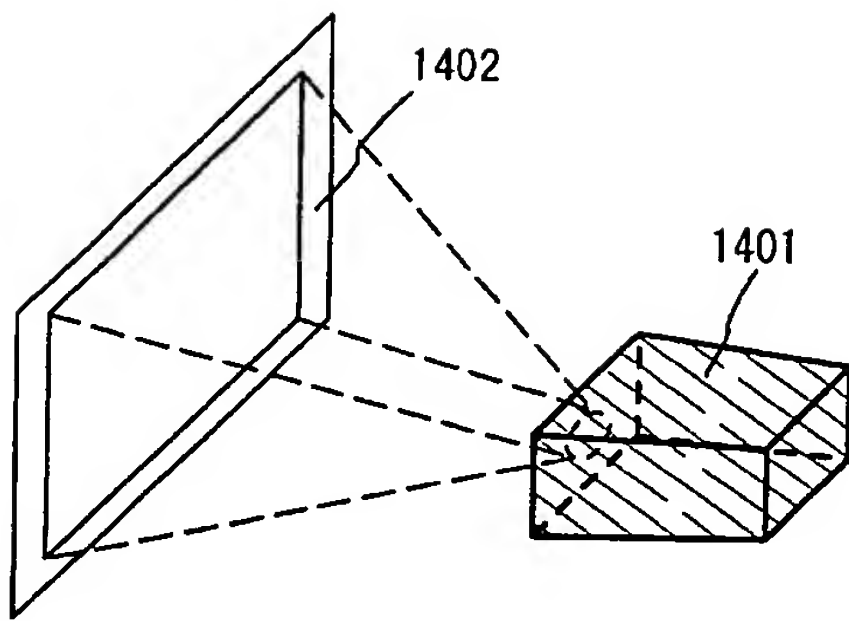


FIG. 15A

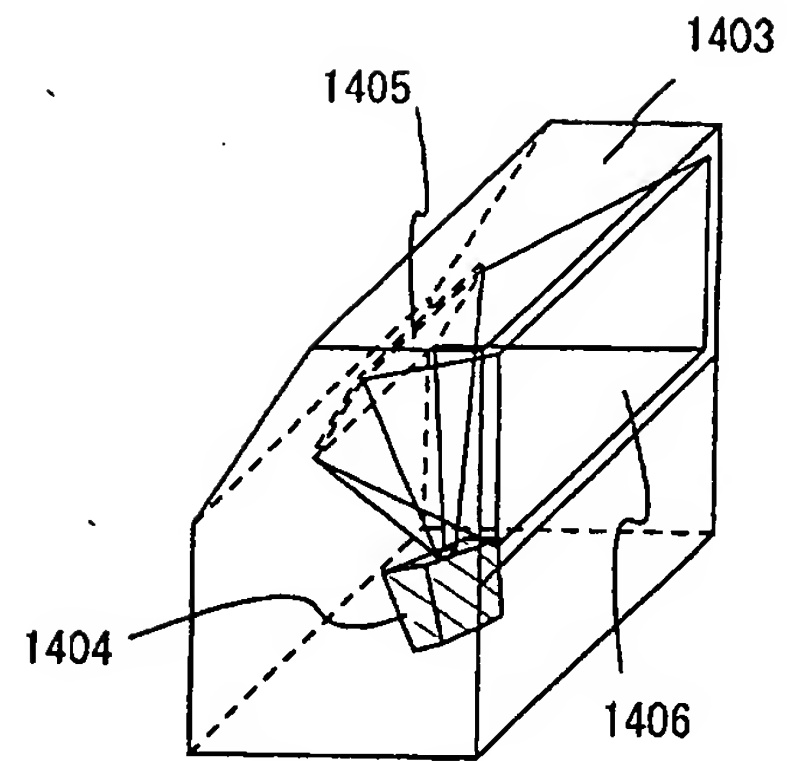
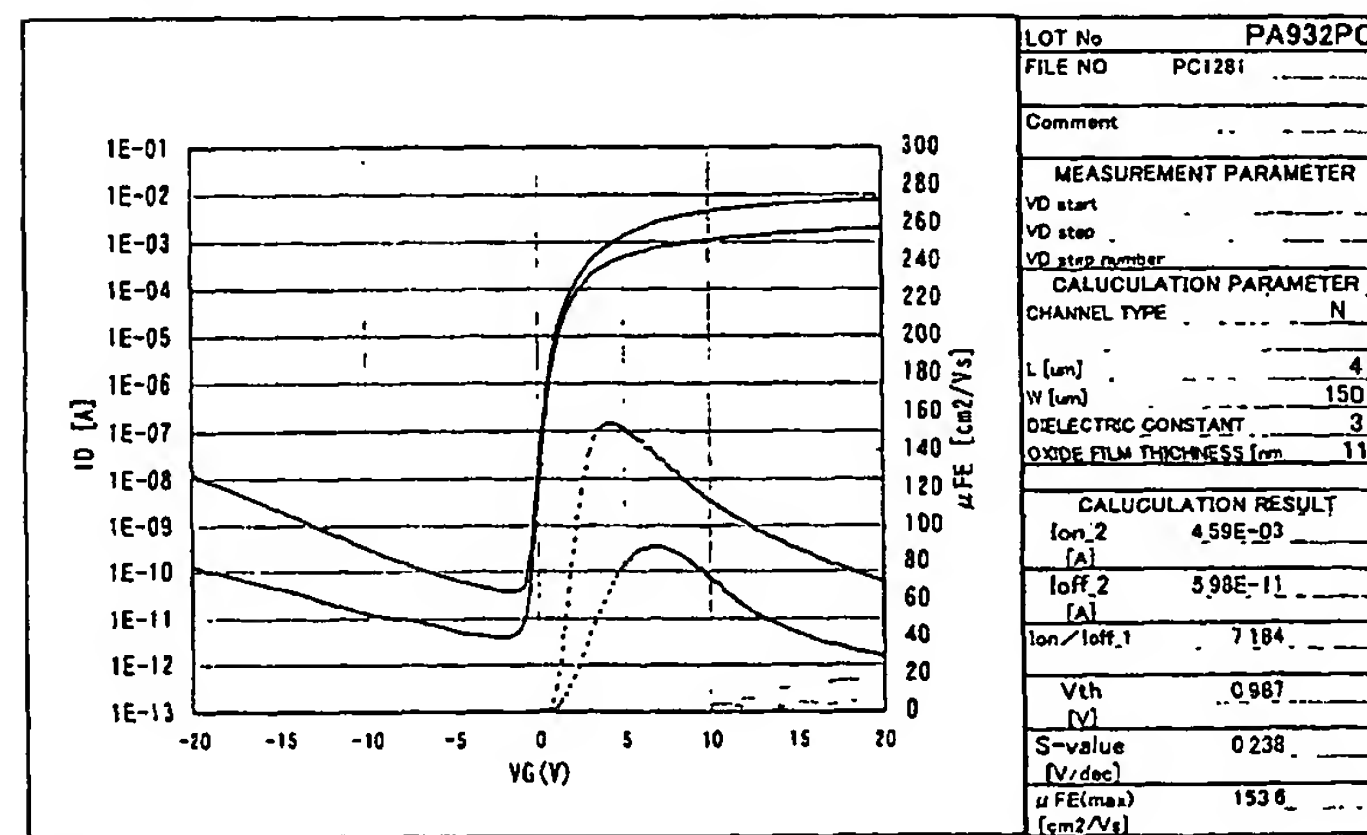
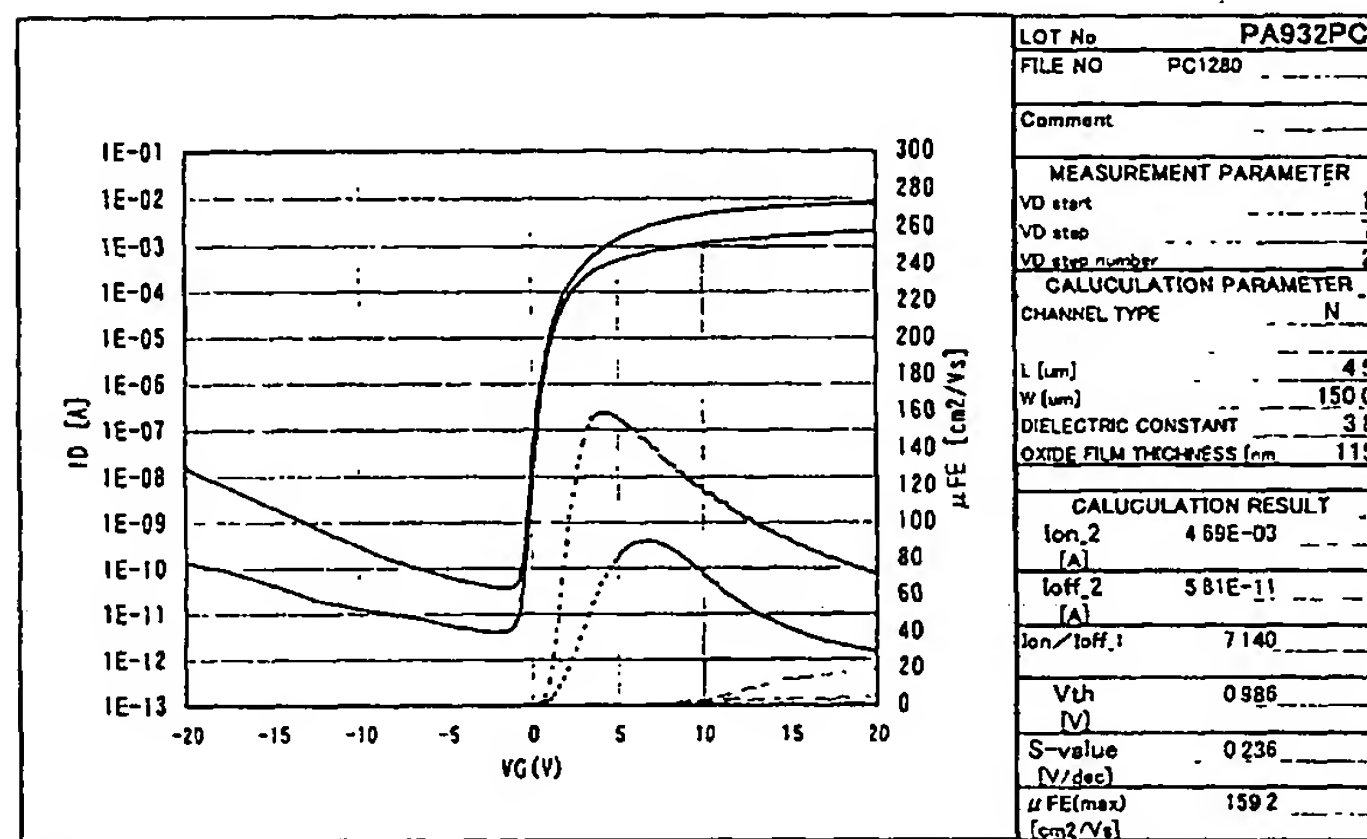


FIG. 15B

1006043-123401



Graph showing the relationship between the gate voltage ( $V_G$ ) and the drain current ( $I_D$ ) for a MOSFET. The x-axis represents  $V_G$  (V) from -20 to 20. The y-axis represents  $I_D$  (A) on a logarithmic scale from  $1E-13$  to  $1E-01$ . The solid line shows the transfer characteristic, and the dashed line shows the output characteristic at  $V_G = 5$  V.



1711 : GATE SIGNAL LINE DRIVING CIRCUIT	1707 : SHIFT REGISTER CIRCUIT	1708 : LEVEL SHIFTER CIRCUIT	1709 : BUFFER CIRCUIT	1712 : SOURCE SIGNAL LINE DRIVING CIRCUIT	
				1702 : SHIFT REGISTER CIRCUIT	
				1703 : LEVEL SHIFTER CIRCUIT	
				1704 : BUFFER CIRCUIT	
				1705 : SAMPLING CIRCUIT	
				1706 : PRE-CHARGE CIRCUIT	
1701 : PIXEL REGION				1710 : PROTECTIVE CIRCUIT	

FIG. 18

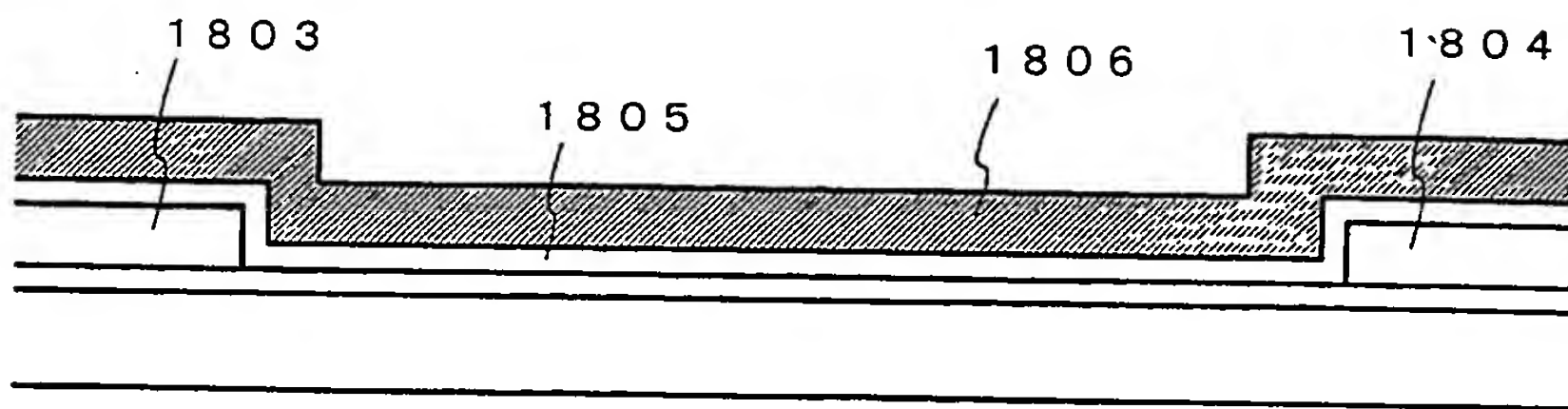


FIG. 19A

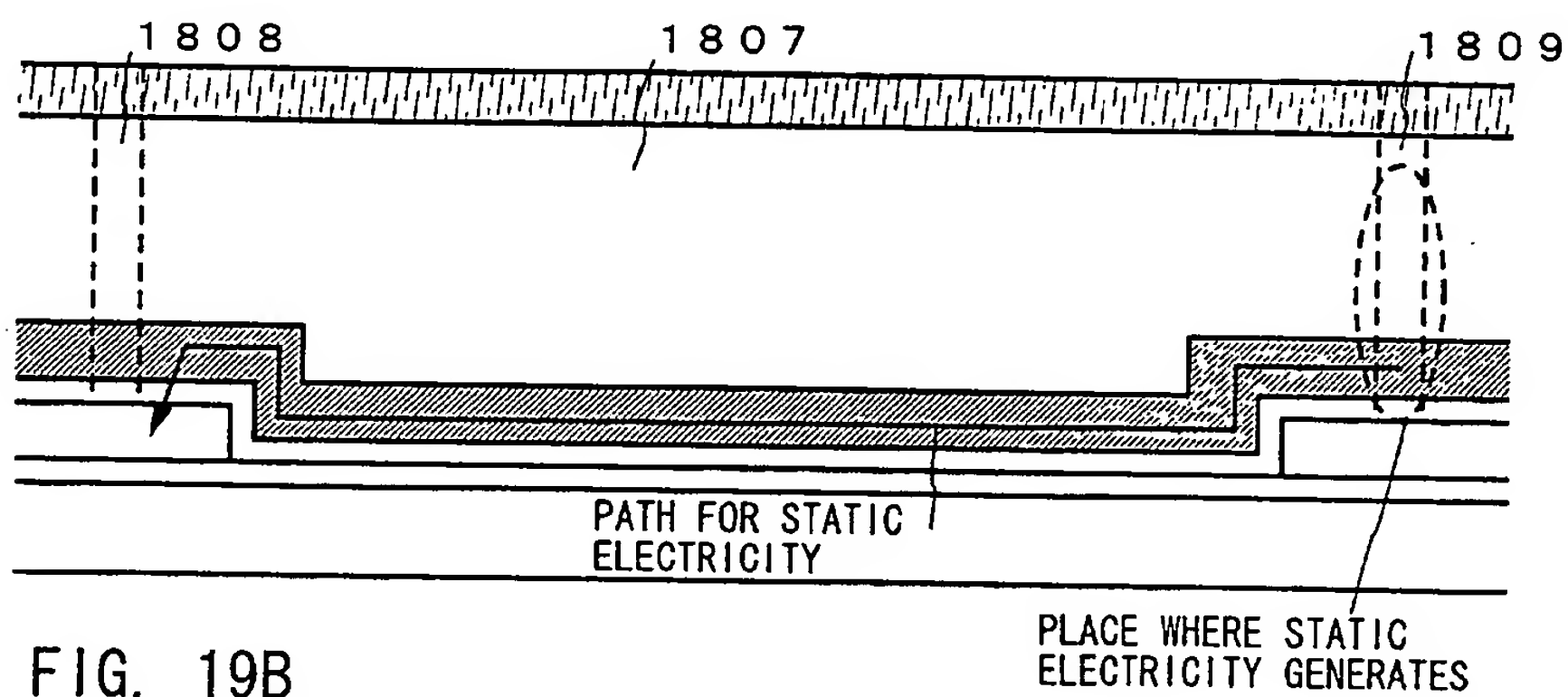


FIG. 19B

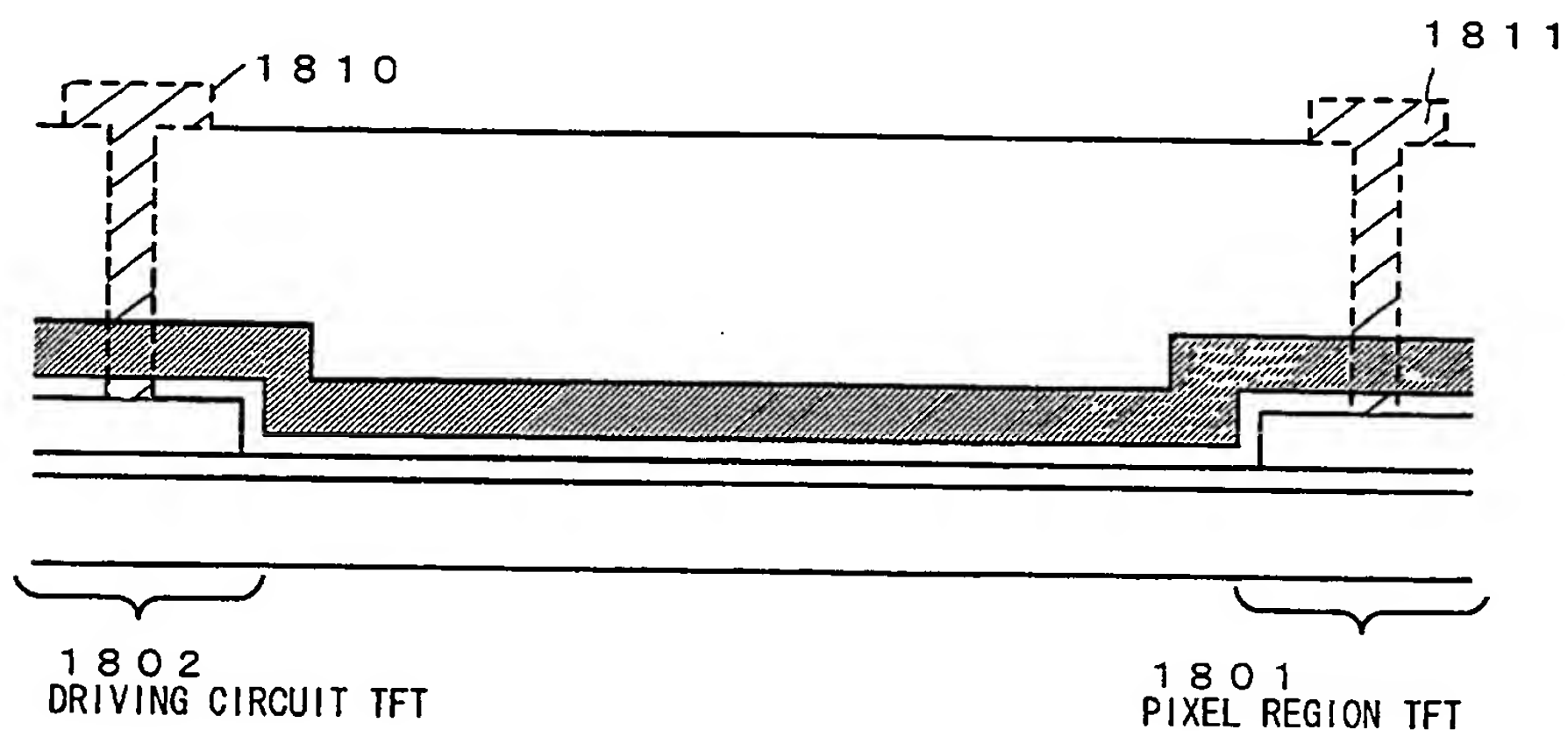


FIG. 19C

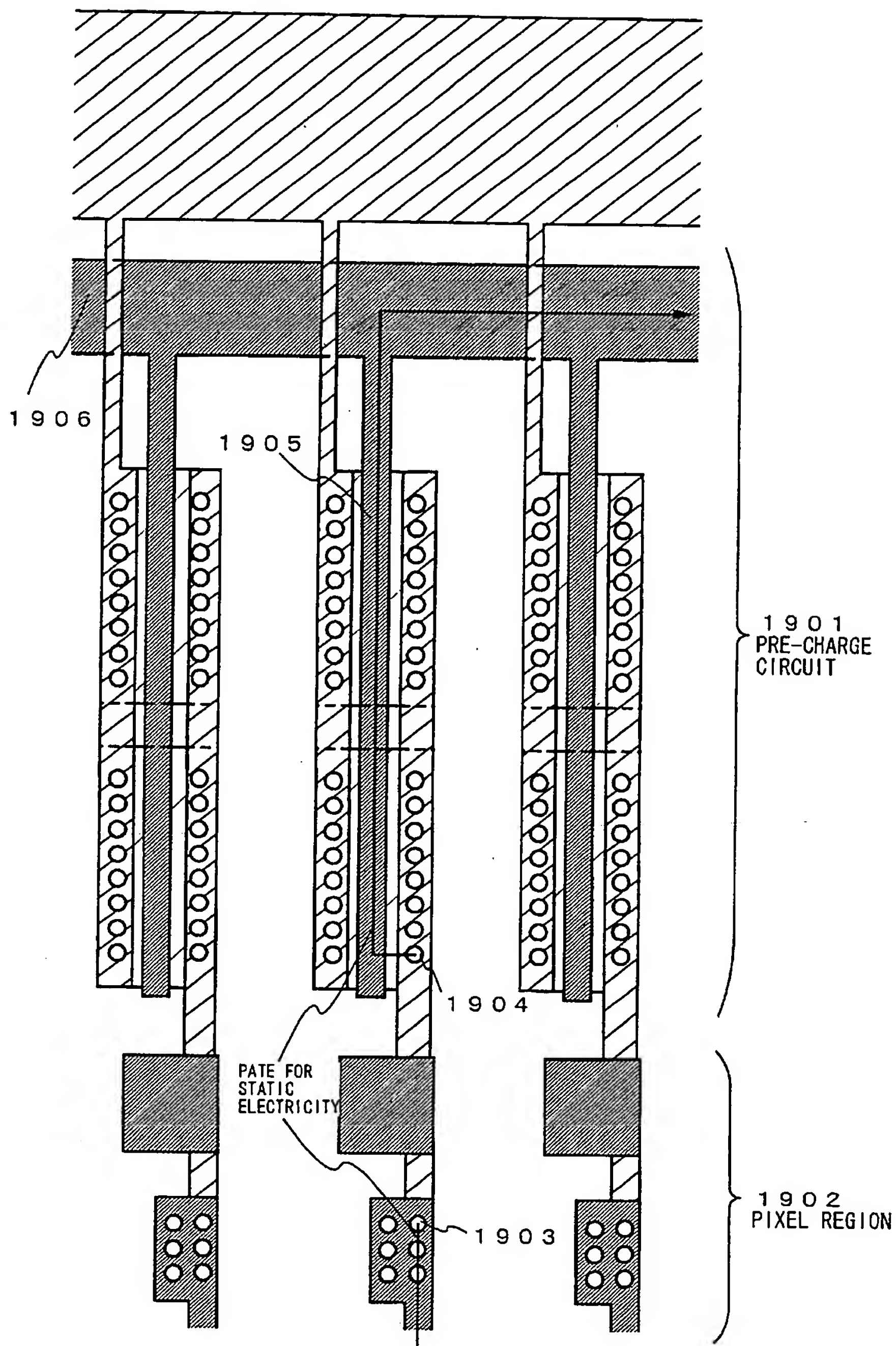


FIG. 20